ABSTRACT OF THE DISCLOSURE

A solid-state imaging device comprising an imaging area having unit cells, a vertical driving circuit, signal processing circuits, a horizontal driving circuit, and an output circuit. Each of the unit cells including first and second photoelectric conversion/storage sections, first and second charge readout circuits, a potential detecting circuit, a reset circuit, and an address circuit. The solid-state imaging device has a first operation mode in which the first and second charge readout circuits are driven at substantially the same timing by the vertical driving circuit, the charges stored in the first and second photoelectric conversion/storage sections are transferred to and added together in the charge detecting section, and the potential detecting circuit detects the added charges, generates and transmits a potential corresponding to an amount of detected charges to the vertical signal line, and outputs the potential from the output circuit via the signal processing circuits.